Application Note 5026
9 April 2008
120-5026-000H

PCB Design with an EM250

For the EM250 SoC Platform

Ember's kit and tool offerings provide a ZigBee product designer a number of paths towards the successful design of an EM250-based ZigBee-compliant solution. The lowest risk path begins with the purchase of an EM250 development kit (with an RF Evaluation Kit, a JumpStart Kit, or a Development Kit). These kits contain software, hardware, and documentation designed for software and hardware developers to develop applications efficiently. In addition, they provide an avenue for customer support and training to further the understanding of Ember's product offerings. Once the design team is familiar with Ember's EM250 and EmberZNet software, the next step in the design path involves designing application specific hardware to meet the product requirements.

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Introduction

Ember recommends the hardware designer familiarize themselves with Ember's EM250 reference designs because several are bundled within the most recent release of EmberZNet Software stack. This variety is intended to meet the design requirements for most ZigBee-based products and allow for a lower risk and simpler design and implementation.

Ember has released the following EM250-based Reference Designs:

- EM250-Based Design with Lattice Balun, 4-Layer *(EM250_REF_DES_LAT.zip)*
- EM250-Based Design with Ceramic Balun, 4-Layer *(EM250_REF_DES_CER.zip)*
- EM250-Based Design with Lattice Balun and +18dBm Power Amplifier, 4-Layer (*EM250_REF_DES_EXT_PA_GBR.zip* and *EM250_REF_DES_EXT_PA_PDF.zip*)
- Low-Cost Version of the EM250-Based Design with Lattice Balun
  - 4-Layer Design, Inverted-F Antenna, 0.062" thick (EM250_REF_DES_LC_LAT_INV-F_62mil.zip)
  - 4-Layer Design, Inverted-F Antenna, 0.8mm thick (EM250_REF_DES_LC_LAT_INV-F_0.8mm.zip)
  - 2-Layer Design, 0.062" thick (EM250_REF_DES_LC_LAT_2LAY_062.zip)
  - 2-Layer Design, 0.040" thick (EM250_REF_DES_LC_LAT_2LAY_040.zip)

Each reference design contains a schematic, bill of materials (BOM), and layout files (Gerber and PDF) that provide guidelines for the schematic capture and PCB design of the ZigBee product.

This application note is intended to accompany the reference designs and provide detailed information of each design. This document is intended to be read by the hardware and test design engineers who are designing the EM250-based PCBs. After reading this document, engineers should be able to successfully implement a design involving the EM250.

EM250 Design Description

Due to the highly integrated nature of the EM250, the primary PCB-level design focus centers on the off-chip components. Figure 1 illustrates the EM250 with its off-chip components. The subsequent sections describe the use and selection of the off-chip components. In addition, design trade-offs for the designer will be highlighted when applicable.

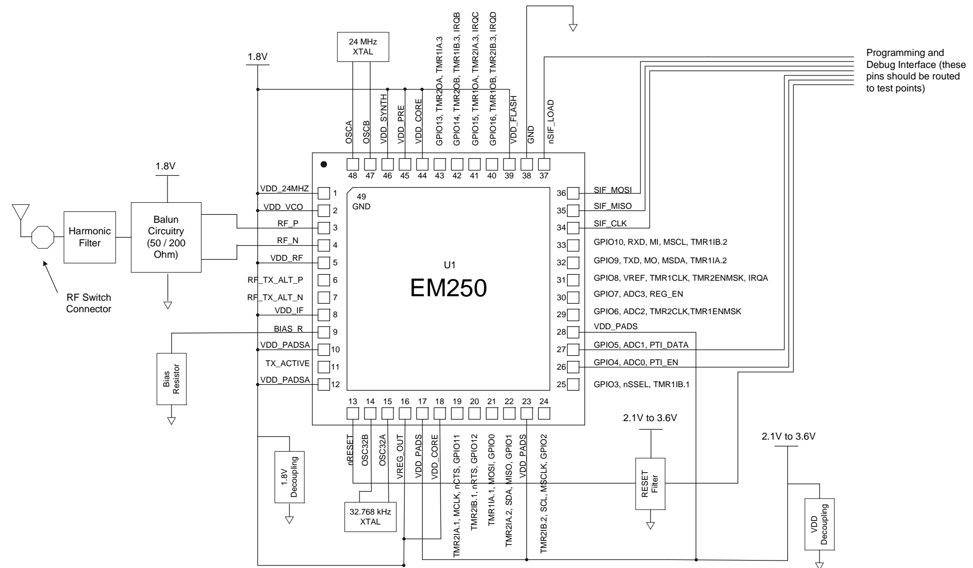


Figure 1. Block diagram of the EM250 reference design

The off-chip components include:

- RF balun circuit (50/200 Ohm)
- Harmonic filter
- Two crystals with loading capacitors
- VDD decoupling capacitors
- VDD plane RC filtering
- Bias resistor
- RC filtering for the asynchronous reset signal

Even though the off-chip component count is small, each component plays an integral role in the overall functionality of the EM250 wireless solution.

Note: The reference designators used within this document refer to components on the EM250 Reference Designs.

A discussion regarding the antenna is beyond the scope of this document, but note that any 50-Ohm unbalanced antenna can be attached to the harmonic filter port. Most antenna manufacturers like Murata, Pulse, and Fractus will tune the antenna to 50 ohms at no cost. The designer will need to add appropriate components for antenna tuning (usually two to three 0402-sized components). Ember recommends you review antenna application notes from the specific manufacturers in order to meet the tuning requirements.

EM250 ZigBee-compliant SOC (U1)

The EM250 integrates an IEEE 802.15.4-2003 transceiver with a 16-bit XAP2b microprocessor, memory, and communication peripherals, as illustrated in Figure 2. The mixed-signal, SOC

comes bundled with EmberZNet, the Ember ZigBee-compliant software, which makes the EM250 a true ZigBee wireless solution.

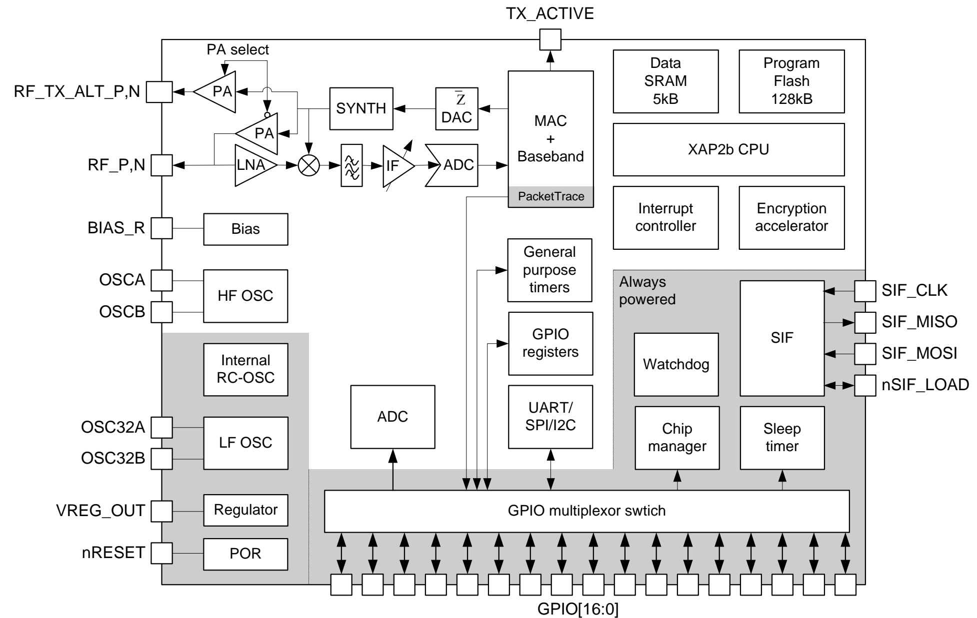


Figure 2. Block diagram of the EM250

The integrated RF analog section contains a direct modulation transmitter with a low IF receiver chain. It allows for two modes of operation, Normal Mode and Boost Mode, which provide the application developer with a trade-off between dynamic range and active current consumption. (The term dynamic range refers to the difference between the RX Sensitivity level and the maximum Radiated TX power from the node.) If the application requires a greater dynamic range for their application, then Boost Mode should be selected as it provides and increase in dynamic range of 3dB at a cost of 5mA.

Note: The application software selects between Normal Mode and Boost Mode by setting a token within the EM250. For more information on the setting of these modes, please refer to the application note *Bringing Up Custom Devices* (120-5031-000).

If the application requires even more dynamic range, the EM250 contains a dedicated TX port (RF_TX_ALT_P/N) to allow easy connection to an external power amplifier (PA). If the application requires an external PA, the designer should use the dedicated TX port for TX mode and the bi-directional port for RX mode. Additional information on this hardware architecture is available in the section Extending the Range of an EM250 in this document, as well as the *EM250 PA Reference Design* available at http://support.ember.com.

The EM250 integrates an IEEE 802.15.4-compliant MAC that supports all lower-level transport activity. In addition, it contains automatic acknowledgement generation and reception,

complex packet filtering, and a packet trace interface for InSight Desktop, providing a true PHY-level packet sniff.

The EM250 contains 128kB of integrated flash, 5kB of integrated RAM, a simulated EEPROM, and a number of application peripherals that target low-power, low-data-rate ZigBee applications. These include:

- 17 general-purpose digital I/O pins
- Two general-purpose 16-bit timers
- 4-single channel/2 differential channel 10-bit ADC
- Serial Controller 1 (UART, SPI, and I^2C)
- Serial Controller 2 (SPI and I^2C)
- Watchdog timer and power-on-reset
- Sleep timer (using either the 32.768kHz or RC oscillator as a source)
- Integrated 1.8V voltage regulator

The EM250 is shipped in a 48-pin, 7x7mm, RoHS-compliant, QFN package. The 49th pin is the metal backplane on the bottom of the package and should be connected directly to PCB ground through an array of vias.

For more information on the EM250, please refer to the *EM250 Datasheet* (120-0082-000).

RF balun (BLN1, L1, L2, L4, L5, R6, C11, C22, and C23)

To improve common-mode noise rejection within the EM250, the integrated RF signal paths (both RX and TX) are differential or balanced (RF_TX_ALT_P and RF_TX_ALT_N are output only while RF_N and RF_P are bi-directional). While the EM250 RX path has a high input impedance (~3k Ohm), the integrated TX power amplifier has been designed to deliver maximum output power when the load impedance approaches 200+j90 Ohm differential. Therefore, the RF balun design is optimized for TX output power instead of the traditional RX input impedance.

Because the RX and TX signals are differential, a RF balun must be implemented to interface to a single-ended (50-Ohm) antenna. The basic design requirements for the balun are:

- The balun must allow a 1.8V DC feed to the integrated PA and LNA within the EM250.
- The balun must be low loss and provide an impedance conversion from 50 Ohms to 200 Ohms.

The balun topology can be either discrete components (lattice, also called LC) or an integrated ceramic balun (both are detailed in the sections that follow). While both provide the required 50/200 Ohm conversion, the discrete balun has a lower loss and slightly lower cost (~$0.05 in high volume). The ceramic balun provides a simpler design that allows for more efficient tuning.

Before starting the design, designers will need to determine which balun topology meets the cost and performance demands of their product. Ember's Reference Designs are grouped by balun architecture. In most cases, the Lattice Balun meets the long-term cost and

performance objectives of the ZigBee-based product. Both the ceramic and LC baluns are available for download at http://support.ember.com.

Ceramic balun (BLN1)

Figure 3 illustrates a schematic of the ceramic balun topology used by the Ember design team. As shown in Figure 3, the only matching component is an inductor (L5) across the balanced port (RF_P and RF_N). This allows for a signal degree of freedom to maximize the TX power supplied to the unbalanced port.

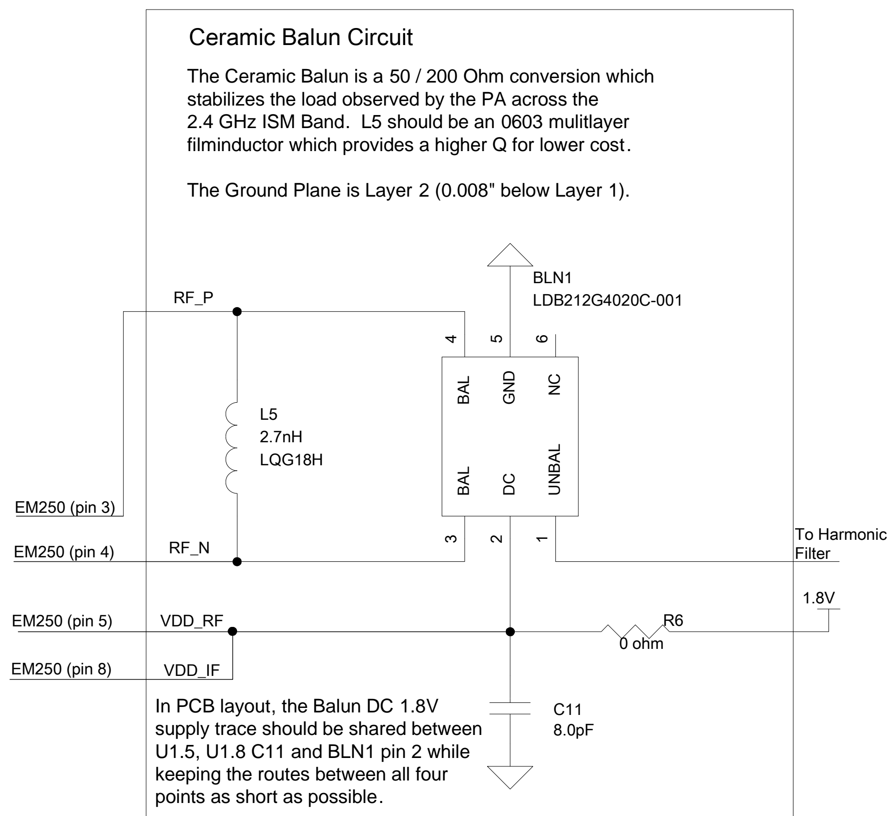


Figure 3. Schematic of RF ceramic balun

As specified in the *Ceramic Balun Reference Design* BOM, Ember recommends using either a Murata (LDB212G4020G-001) or a TDK (HHM1521) 50 to 200 Ohm ceramic balun for BLN1 along with a 2.7 nH, multilayer, 0603 inductor for L5. For compact designs or for designs that use an external PA and require two baluns, a 0402 wire-wound inductor may be substituted. Using a different inductor type will cause the inductor value to change. L5 can be adjusted up or down in value until maximum transmit power is achieved. Typical values would be somewhere in the 2 nH to 6 nH range.

To reduce the chance of needing to tune the value of L5, the balun and inductor should be placed as close to pins 3 and 4 as possible. Following the reference design layout as close as possible in this area will also help. The differential input to the balun is approximately 200

Ohms, but since a 200 Ohm differential line is extremely thin for manufacturing tolerances, these lines are not required to be 200 Ohms. As long as these lines are short, the inductor will compensate for this.

For maximum sensitivity, pins 3, 4, 5, and 8 should be as close to the same potential as possible, therefore the balun DC feed should be tied to C11 and pins 5 and 8 with as short a trace as possible.

To reduce die size, the integrated PA and LNA within the EM250 require a DC power feed. This DC power feed is coupled from the balun. Therefore, the 1.8V (VDD_CORE) needs to be connected through the balun. This is shown in Figure 3.

Lattice (LC) balun

Figure 4 illustrates a schematic of the lattice balun topology used by the Ember design team. The lattice balun contains two LC circuits on the differential port (L1 – C22 and L4 – C26) along with a DC coupling inductor (L2), and DC blocking capacitor C23. To avoid the balun requiring tuning, the balun should be as compact and close to the EM250 as possible. Traces to pins 3 and 4 do not need to be 200 Ohms. L2 can be changed from a 0603 multilayer inductor to a 0402 wire wound inductor, but this will require the value to change.

If tuning is required, change the value of L2 until maximum transmit power is achieved. This value will typically be in the 2 nH to 6 nH range. Once this inductor’s value is optimized, extra performance may be had by tweaking C23. Typical values are 1 pF to 3 pF.

To minimize EVM, the 0.75pF capacitance value for C22 and C26 must be held. This capacitance resonates with the bond wire and parasitic inductance within the EM250 to allow for the optimal TX performance. Ember recommends not altering the values of L1, L4, C22, or C26.

DC power should be connected between pins 5 and 8 and the balun DC feed with as short a trace as possible to maximize sensitivity.

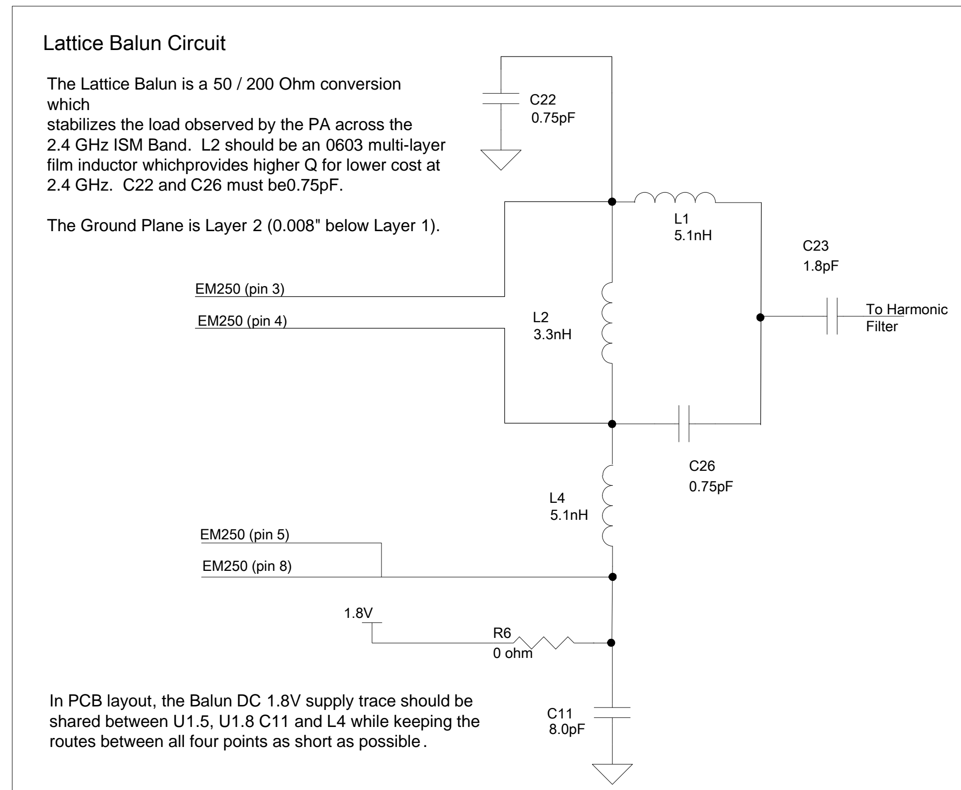
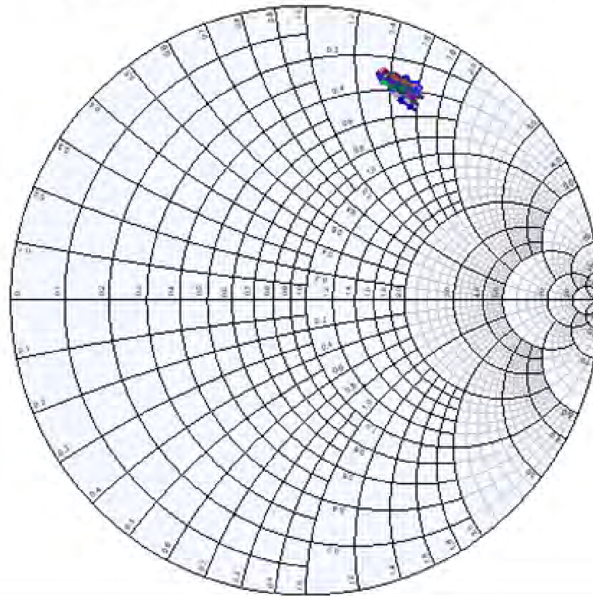


Figure 4. Schematic of the lattice balun topology

Custom balun design

Alternate 50/200 Ohm balun topologies can be used. The balun should be designed to present the optimum impedance for maximum power and sensitivity. The optimum impedance that should be presented to the RF port was derived using simulations of the lattice balun and took into account parasitics and board effects. This impedance is shown in Figure 5. It is the same for both the RF port and the RF ALT port, for both transmit and receive modes. (Note that this is the gamma optimum of the transmitter and receiver. When the balun is connected to the chip, the 50-Ohm port of the balun output will not look like 50 Ohms.)

Optimum Load, Monte Carlo Simulation



S11

# MHz S MA R 50		
Frequency	**Magnitude**	**Degrees**
2405	0.792962	67.0032
2415	0.792441	66.5579
2425	0.791920	66.1160
2435	0.791401	65.6776
2445	0.790888	65.2426
2455	0.790381	64.8111
2465	0.789884	64.3830
2475	0.789397	63.9583
2485	0.788924	63.5371

Simplified Diagran of Otimum Load Simulation

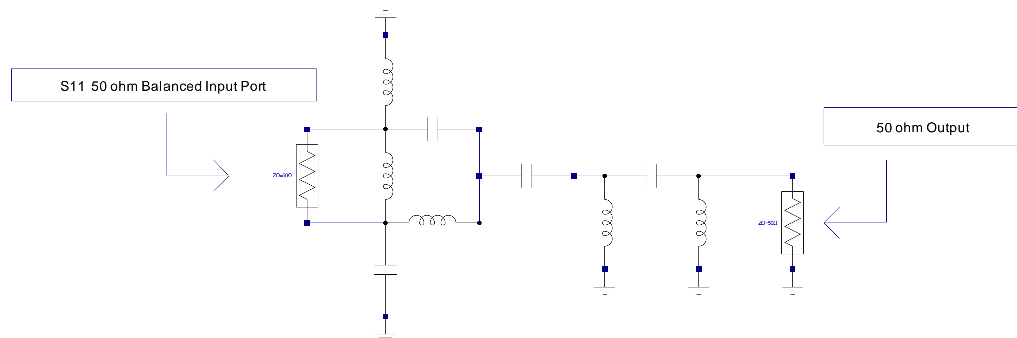


Figure 5. Optimum load impedance

Harmonic filter (L6, C24, and C25)

The EM250 has been designed to exceed FCC and ETSI regulations for wireless communications. However, to provide adequate margin over the conducted 2nd harmonic requirement (50dBuV/m at 3m), a harmonic filter is required. This is shown as L6, C24, and C25 in Figure 6. Alternately, a 50-Ohm ceramic filter can also be used.

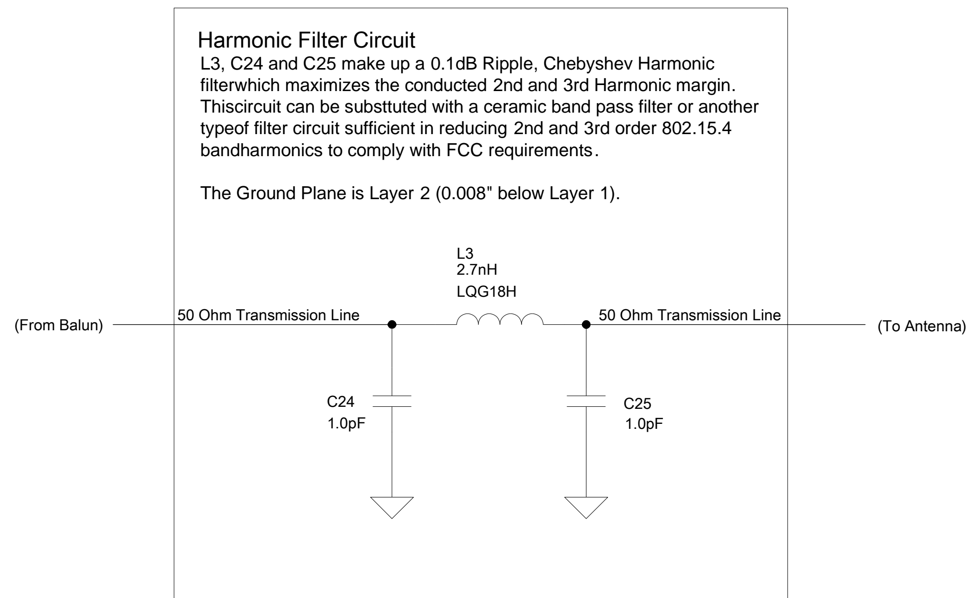


Figure 6. Harmonic filter circuit

Figure 7 illustrates the Monte Carlo analysis of the harmonic filter.

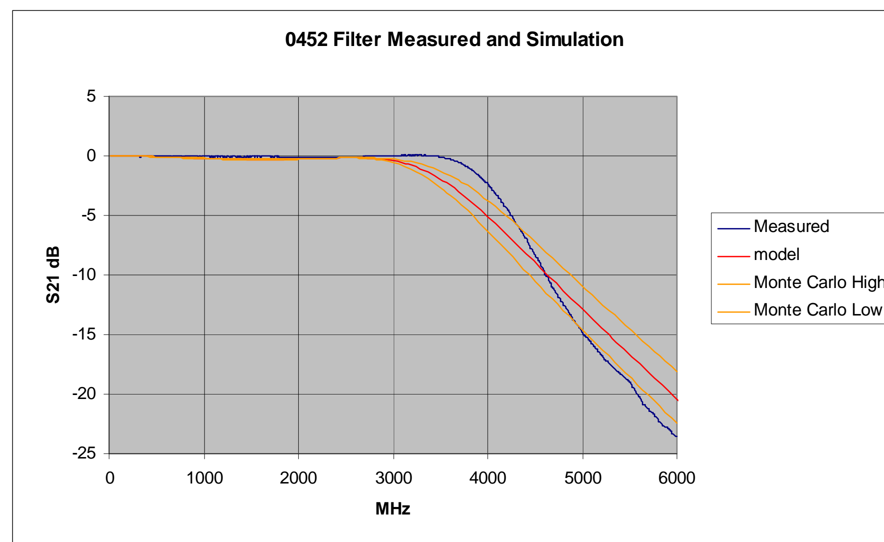


Figure 7. Harmonic filter response

High-frequency crystal reference (Y1, C7, C8, and R3)

The EM250 requires a single, accurate 24MHz crystal source in order to develop the proper EM250 clock distribution and IEEE 802.15.4 timing (see Figure 8).

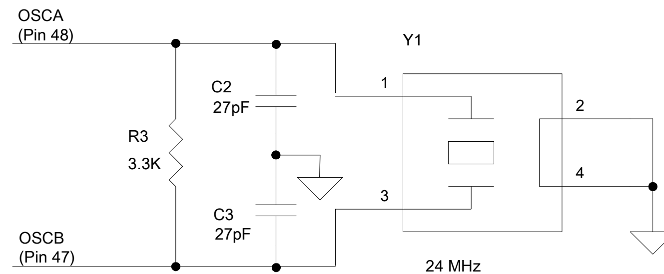


Figure 8. 24MHz high-frequency crystal

The 3.3 Kohm resistor is required for two reasons:

- An internal crystal bias setting sets the crystal drive level of the 24MHz crystal. This bias setting is calibrated to be the lowest possible level for stable oscillation. (The lower the setting, the lower the current consumption.) The bias calibration occurs at power up. As the crystal drive level increases, the oscillator signal level increases. A high signal level will pull the 24MHz oscillation frequency toward the +/- 40ppm limit. Adding a 3.3k Ohm shunt resistor prevents frequency pulling over the allowable the crystal drive levels.
- The ESR tolerance causes a wide spread of ESR values across multiple reels of parts. The shunt resistor improves the ESR tolerance of the crystal and prevents a situation where the ESR gets too low. If the ESR is too low, then larger signal swings for the same bias current are present. Larger signal swings increase the risk of cloc- related noise interferers within the EM250.

Ember testing demonstrated 3.3 Kohms is a good choice for the value of the resistance.

Ember recommends that the shunt capacitors be located fairly close together and share a common ground via. The shunt capacitors and the crystal form a resonant circuit with a reasonably high Q, so the circulating currents are high. As a result, despite only consuming 1mA (for example), the circulating current through the shunt caps may be several mA. If the grounds of the capacitors are widely separated, this several mA loop current has to flow through the ground plane to get between the two capacitors. The high current causes voltage to be developed due to the via inductance, as well as potentially inducing a voltage in the ground plane. Bringing the capacitors together means the majority of the loop current flows in surface tracks—only imbalance current flows to ground, which should be small if the signal across the crystal is symmetric and sinusoidal. Whether this really makes a difference or not is difficult to say, and capacitors are commonly taken to ground separately. However, the crystal is very near the RF and the VCO in particular, and 24MHz tones of the VCO are very detrimental, so the problem is best avoided.

Due to the timing requirements of the IEEE 802.15.4-2003 Standard, this crystal must meet an accuracy of +/-40ppm over tolerance, temperature, and aging as listed in Table 1. In addition, the crystal must have a maximum ESR of 60 Ohms to control the integrated oscillator signal strengths. To stabilize the ESR over multiple drive levels, Ember recommends using a shunt resistor (R11) across the crystal drive ports.

A manufacturing token within the EM250 stores the crystal bias register setting. This setting is automatically determined during PCB manufacturing test when Ember's RangeTest or MFG Library SW is used, and it is dependent upon the crystal chosen. For more information on this token, refer to the application note *Bringing Up Custom Devices* (120-5031-000). Loading capacitors C7 and C8 should be chosen according to the crystal manufacturer's requirements.

Table 1. High Frequency Crystal Requirements

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Frequency			24		MHz
Duty cycle		40		60	%
Phase noise from 1kHz to 100kHz				- 120	dBc/Hz
Accuracy	Initial, temperature, and aging	- 40		+ 40	ppm
Crystal ESR	Load capacitance of 10pF			100	Ω
Crystal ESR	Load capacitance of 18pF			60	Ω
Start-up time to stable clock (max. bias)				1	ms
Start-up time to stable clock (optimum bias)				2	ms

Optional low-frequency crystal reference (Y2, C21 and C22)

The EM250 contains an integrated sleep timer which allows for SW configuration of sleep/wake cycles of the wireless node. There are two options for driving the sleep timer: a 32.768 kHz crystal oscillator or an internal RC oscillator. The crystal oscillator is more accurate but consumes more current than the RC oscillator. The RC oscillator is sufficient for operating Ember's EmberZNet stack. Therefore, the application's sleep timing accuracy will decide if a 32kHz crystal is required.

Figure 9 illustrates the crystal oscillator with its loading capacitors. To reduce the effects of overdriving the oscillator circuit within the EM250, Ember recommends an asymmetrical loading of the crystal.

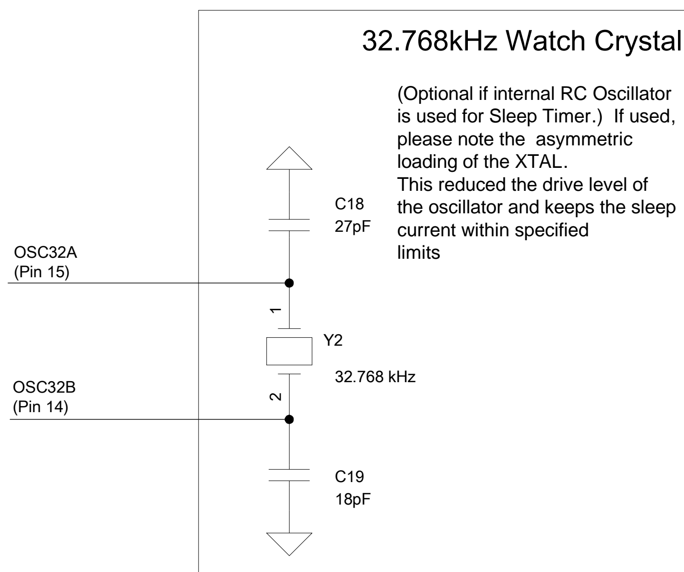


Figure 9. 32kHz low-frequency crystal

If the application does not need the 32kHz crystal, then the pins OSC32A and OSC32B can be left unconnected.

RBIAS (R8)

The EM250 requires a single, accurate (+/-1%) resistor to set the current references for the power management block within the EM250. The value of this resistor must be 169k Ohm, 1% tolerant resistor.

nRESET noise filter (R1 and C1)

To reduce static noise coupled onto the unshielded InSight port cable, a simple RC filter is added to the asynchronous nRESET signal. Figure 10 shows this filter.

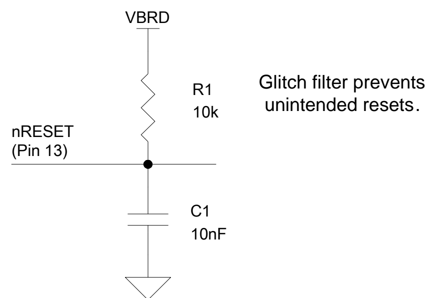


Figure 10. Reset noise filter

Ember recommends the pull-up resistor be 10k Ohm, 5% tolerant, while the shunt capacitor should be 10nF, 5% tolerant. When the external filter is used in conjunction with the integrated power-on-reset delay, an asynchronous, external reset must be asserted (low) for longer than 500ns before the EM250 latches the reset event.

1.8V Regulator load capacitor

The EM250 operates over a supply voltage (VBRD) of 2.1 to 3.6V. An integrated 1.8V regulator converts VBRD down to 1.8V. To stabilize the integrated regulator, a 10uF tantalum loading capacitor is required on the output of VREG_OUT (Pin 16) of the EM250. A series resistor (R7) is used to keep the minimum ESR of the loading capacitor below 1 Ohm. This is shown in Figure 11.

The tantalum capacitor can be replaced with a ceramic capacitor. The value or the series resistor may need to be adjusted to compensate for the difference in ESR.

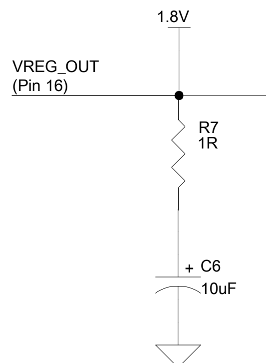


Figure 11. 1.8V regulator loading capacitance

1.8V Net decoupling

To minimize noise and coupling paths into the EM250, decoupling capacitance must be placed on each of the VDD pins, as shown in Figure 12.

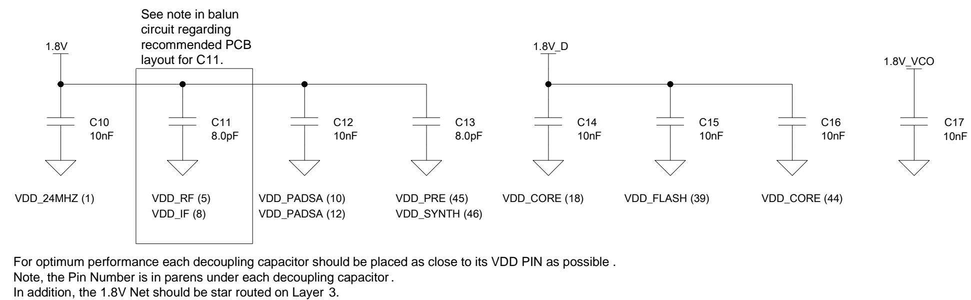


Figure 12. VDD decoupling for the EM250

All decoupling capacitors should be placed as close to the EM250 as possible as well as in between the source point (via) and the EM250 pin. In addition, all values should be maintained as defined by the *EM250 Reference Design*.

Digital 1.8V filtering

To keep the Radio Active current at 36mA, Ember recommends the addition of a single element filter (resistor) between the digital and analog 1.8V nets, 1.8V and 1.8V_D, respectively (see Figure 13). This resistor maintains a reduced bias current for the digital logic within the EM250. If this resistor is not used, the RX current will increase by 1mA to 37mA.

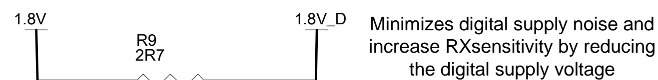


Figure 13. Digital VDD filter

The lower current consumption also allows for a reduction in the digital 1.8V Domain noise. This means the RX Sensitivity improves by 2dB with the 2.7 Ohm resistor.

Test connector (J3)

In order to assist with manufacturing test of the printed circuit assemblies, Ember recommends the use of a RF switch connector. The ceramic and external PA designs use the MC-Card RF switch connector (J3). The lattice designs use the Murata RF switch connector (J3).

The RF switch connector allows an external 50 Ohm, RF cable to be connected during PCA testing. With the external RF cable connected to the RF switch connector, the antenna is isolated from the RF test measurement which provides for an accurate and repeatable RF Test. When the cable is not connected, the RF switch connector allows the antenna to be connected to the EM250 RF path.

The RF switch connector is in stock, low cost, and low loss. However, if a designer does not want to incur the extra cost, they can add the footprint for the RF switch connector along

with two resistors to select the connector during prototyping phase and not populate when in higher volume manufacturing.

Debug and programming interface

In order to program the integrated flash and debug the software application within the EM250, a synchronous serial interface, known as SIF, connects either Ember's InSight Adapter (ISA) or Ember's USB Link Programmer directly to the XAP2b core and integrated memory bus. The SIF is a synchronous port which operates in a similar command/response manner as JTAG. It uses four, dedicated pins (SIF_CLK, SIF_MISO, SIF_MOSI and nSIF_LOAD) from the EM250.

To facilitate packet-level debugging of an EM250-based application, Ember utilizes two GPIOs, GPIO4 and GPIO5, as well as nRESET. To use the full program and debug environment from Ember's tool chain (InSight Desktop), Ember recommends the designer route the following signals from the EM250 to either test points or to a connector:

- nRESET
- GPIO4
- GPIO5
- SIF_MOSI
- SIF_MISO
- SIF_CLK
- nSIF_LOAD
- VDD (2.1V to 3.6V)
- GND

To allow for direct connection to Ember's InSight Adapter and InSight USB Link Programmer with the InSight Port cable, the designer should consider using a dual-row, 0.05" pitch connector similar to the one used on the EM250 radio communication module (RCM).

The connector used on Ember's EM250 Radio Communication Module (RCM) is from Samtec (MFG P/N: FTSH-105-01-F-DV-K). It is keyed to guarantee proper connection with the InSight Port cable (Samtec P/N: FFSD-05-D-12.00-01-N). Figure 14 illustrates the pinout for the InSight Port, and

Table 2 describes the pins.

Figure 14. InSight Port pinout

Table 2. Insight Port Pins

Pin #	Signal Name	Direction	Description
1	VBRD	Power	2.1 to 3.6V supply for the RCM
2	SIF_MISO	Output	Serial interface, master in, slave out
3	SDBG	Output	Debug signal to be used on future pin-compatible products
4	SIF_MOSI	Input	Serial interface, master out, slave in (An external pull down resistor should be added to SIF_MOSI to guarantee state of pin in Deep Sleep mode)
5	GND	Power	Ground
6	SIF_CLK	Input	Serial interface, clock (internal pull-down within EM250)
7	nSIF_LOAD	I/O	Serial interface, load strobe (open collector with internal pull-up within EM250 (In order to strengthen the pull-up, and external pull-up should be added in noisy environments.)
8	nRESET	Input	Active low, EM250 reset (internal pull-up within EM250)
9	PTI_EN (GPIO4)	Output	Packet trace frame signal
10	PTI_DATA (GPIO5)	Output	Packet trace data signal; 500kbps

To assist customers with their manufacturing and prototyping needs, Ember has developed programming solutions with gang programmers as well as multi-stage USB Link programmers. For more information on different programming options, please contact Ember Support (support@ember.com).

Connecting the EM250 to a host microprocessor using the SPI interface

In certain situations you may want to connect an EM250 to a host microprocessor using the SPI interface. Table 3 shows how to map the SPI interface from the EM260 to the EM250.

Table 3. SPI Connections

EM260 SPI Connections		ATmega 32L SPI Connections		EM250 SPI Connections	
EM260 Pin Number	**EM260 Pin Name**	**AVR32 Pin Number**	**AVR32 Pin Name**	**EM250 Pin Number**	**EM250 Pin Name**
17	MOSI	1	MOSI	21	GPIO0
18	MISO	2	MISO	22	GPIO1
20	SCLK	3	SCK	24	GPIO2
21	nSSEL	44	nSS	25	GPIO3
15	nSSEL_INT	44	nSS	19	GPIO11
25	nHOST_INT	11	INT0	33	GPIO10
35	nWAKE	43	OC0	42	GPIO14
11	nRESET	41	T1	13	nRESET

Extending the Range of an EM250

As previously stated, an external power amplifier (PA) can be added to an EM250-based design to extend the overall communication range. The EM250 contains a dedicated TX port (RF_TX_ALT_P/N) to allow easy connection to an external PA. Figure 15 illustrates a block diagram for the external PA connection.

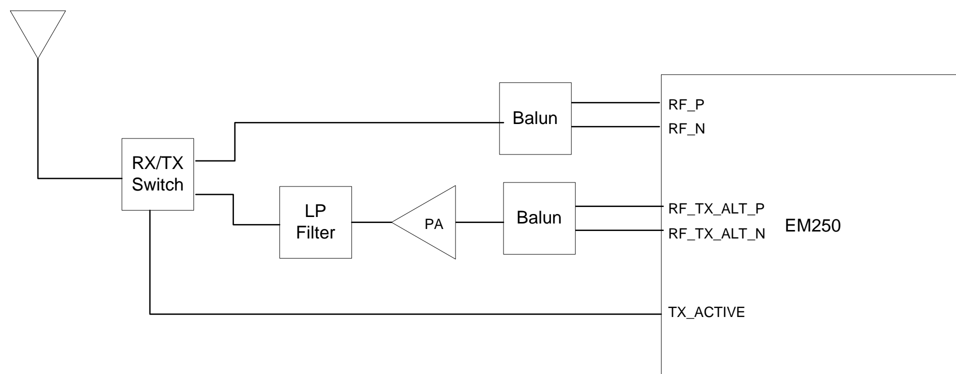


Figure 15. Block diagram of an EM250 with a PA

As shown in Figure 15, there are dedicated TX and RX signal paths to the EM250. The TX path contains the external power amplifier as well as the harmonic filter. Each path contains an RF balun. The balun can be either the lattice or the ceramic balun as described in the RF balun (BLN1, L1, L2, L4, L5, R6, C11, C22, and C23) section. It is important for the designer to use the appropriate balun for their performance and cost requirements.

Due to the time domain duplex (TDD) nature of ZigBee, a RX/TX switch is required to toggle between the two RF paths (RX and TX). To meet the MAC timing requirements of IEEE 802.15.4-2003, the EM250 drives a digital control line to assist with switching between TX and RX paths (TX_ACTIVE). This active high signal provides 1.8V signal level to the external logic. Because most low-cost RF switching requires two digital control lines, an external inverter

will be required to drive the positive/negative logic. In addition, Ember recommends an open-drain buffer on TX_ACTIVE in order to meet the voltage level requirements of the RF switch logic. Figure 16 demonstrates a timing diagram of the TX_ACTIVE signal.

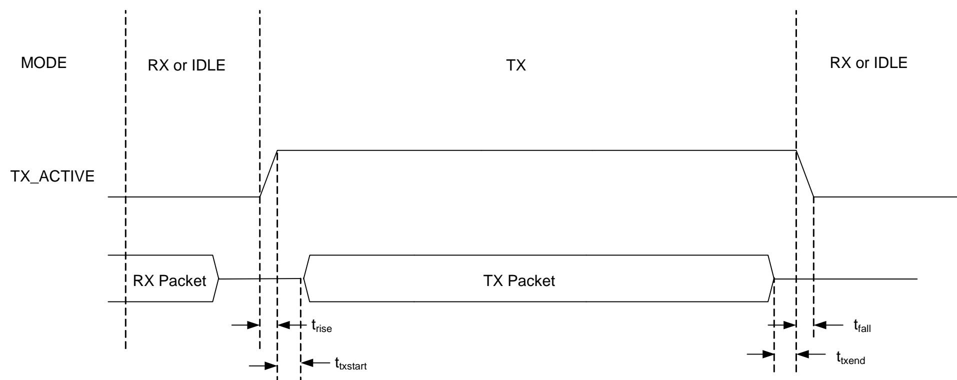


Figure 16. TX_Active timing diagram

Table 4 lists the typical timing requirements of the TX_ACTIVE signal. The designer should make sure the PA and RX/TX switch can meet the timing requirements imposed by this signal.

Table 4. Timing Requirements of the TX_ACTIVE sSgnal

Parameter	Min.	Typ.	Max.	Units
t_{rise}		2		µs
$t_{txstart}$		20		µs
t_{txend}		20		µs
t_{fall}		2		µs

In addition to adding a PA, a customer can add an external low noise amplifier (LNA) in the RX path to further extend the range of the EM250. This is shown in Figure 17. Because of the performance of the EM250 in RX mode in Boost Mode (-99dBm RX sensitivity), and the theoretical limit of receiving a ZigBee packet (-104dBm), there are minimal benefits for adding a LNA to extend the range, and it is not recommended for customers who are concerned about battery life or the cost of their ZigBee device. In addition, Ember does not have a Reference Design with an LNA.

For those wishing to add an LNA, the EM250 receiver had a nominal noise figure design target of 10dB (including balun losses). Thermal noise floor is at -174dBm/Hz, so total noise referred to the receiver input is at -164dBm/Hz. The noise bandwidth of the matched filter is about 1.2MHz, so receiver input noise in this bandwidth is 10*log(1.2e6) bigger, that is, approximately -103dBm/Hz. About 3dB SNR is needed to achieve the 1% PER, so signals at -100dBm should be detectable.

Adding an LNA could improve the sensitivity. It is very possible to achieve under 2dB noise figure in a bipolar-based external LNA. If its gain is much greater than the 10dB receiver noise figure, for example 15dB, it will dominate the overall noise figure. An overall figure of 3dB should be possible. This will extend the sensitivity achievable to
-107dBm.

To add an external LNA, you will need to add an external SP2T switch. The loss of the switch would add directly to the noise figure; for example, a 1dB loss would increase the overall receiver noise figure by 1dB. You can use the Friis formula for cascaded noise factor to see the overall effect:

$$F_{total} = F1 + ((F2 - 1)/G1) + ((F3 - 1)/(G1*G2)) + \ldots$$

Noted that the level of signals hitting the receiver will be higher by the gain of the external LNA. The receiver has been designed as a complete system to meet a set of sensitivity and interference rejection requirements that are mutually conflicting with respect to receiver gain. The net effect will be that the receiver's ability to cope with loud WiFi signals will be reduced by the LNA gain.

When combining an LNA with a PA, and placing nodes in close proximity to each other, it is possible to overdrive the internal receiver, which causes a degradation in performance.

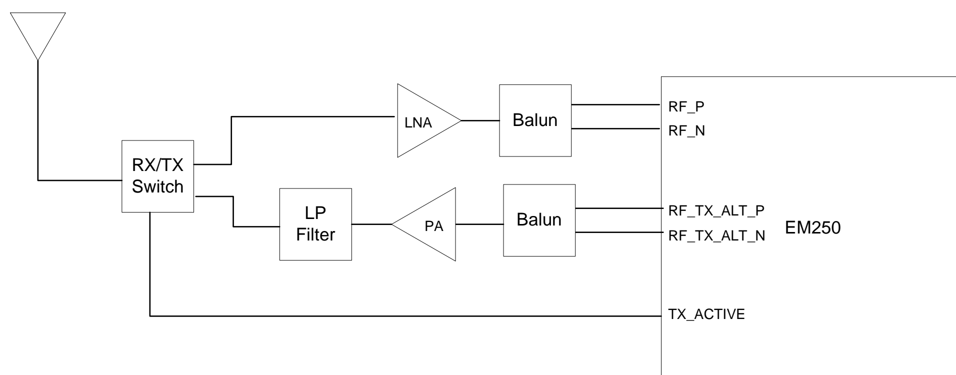


Figure 17. Block diagram illustrating an external PA and LNA

EM250 Low-Cost Designs

Some EM250-based ZigBee applications require the lowest possible Bill of Material cost for the design. Fortunately, there are ways to reduce the cost of an EM250-based design, such as:

- Reduce the number of external components
- Use lower cost components

The trade-off for the lower cost includes a greater height requirement for the components, a reduction in the design flexibility, and reduced overall performance. Ember has released a series of low-cost reference designs for cost-sensitive applications, and this section describes the design trade-offs to achieve the lower cost.

The released EM250, Low Cost reference designs include:

- 4-Layer Design, PCB Antenna 0.062″ thick (EM250_REF_DES_LC_LAT-INV-F_62mil.zip)
- 4-Layer Design, PCB Antenna 0.8mm thick (EM250_REF_DES_LC_LAT-INV-F_0.8mm.zip)
- 2-Layer Design, 0.062″ thick (EM250_REF_DES_LC_LAT_2LAY_062.zip)
- 2-Layer Design, 0.040″ thick (EM250_REF_DES_LC_LAT_2LAY_040.zip)

All of these designs implement an EM250 with a Lattice Balun. The 4-layer designs contain a 0.008″ separation between layers 1 and 2 (GND) for the controlled impedance of the RF microstrip. They also use an inverted-F PCB antenna, and larger lower-cost crystals.

The 2-layer designs keep the ground spacing at 0.062″ and 0.040″ from the top layer. At this thickness, 50-Ohm line becomes too wide to implement effectively. The differences in trace impedance can be compensated for by retuning the balun.

Reduction in external components

The 2-layer versions of the low cost designs have a reduction in the number of decoupling capacitors on the 1.8V and VDD_PADS nets. The reduction in decoupling has a minimal effect on the overall cost reduction, but in high volumes, every little bit helps.

Figure 18 illustrates the reduced decoupling for the 2-layer versions.

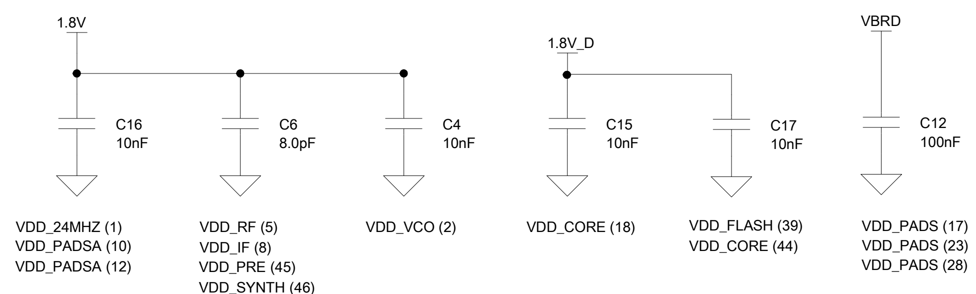


Figure 18. Two-layer, low-cost decoupling

Reduced cost components

In addition, the reduced number of components in the low-cost designs utilize some lower-cost components. The High Frequency crystal on the 4-layer design is implemented with an ECS series crystal from Abracon which reduces the crystal cost by 50% (when compared to the lattice balun reference design).

The ceramic antennas in the 4-layer designs have also been replaced with inverted-F antennas. This antenna takes up more board area than a ceramic antenna. However, on boards with room to spare, significant cost savings can be achieved by printing the antenna.

Due to the fact the 2-layer design achieves the design on two layers of FR-4 substrate, the overall PCB Cost is reduced by 50%.

Low-cost design performance

Ember measured minimal performance (RF, active current or deep sleep current) difference when comparing the 4-layer EM250 Lattice design against the 4-layer EM250 Low Cost Lattice Design (FCC testing is pending). The inverted-F antenna performance is described in the application note *Designing with an Inverted-F PCB Antenna* (120-5052-000).

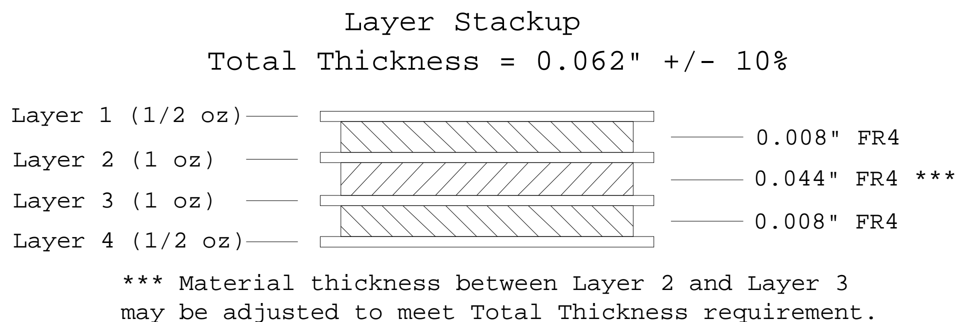
The two layer EM250 design has a 1-dB RF Degradation in RX Sensitivity, but is equivalent in the TX Power.

EM250 Layout Considerations

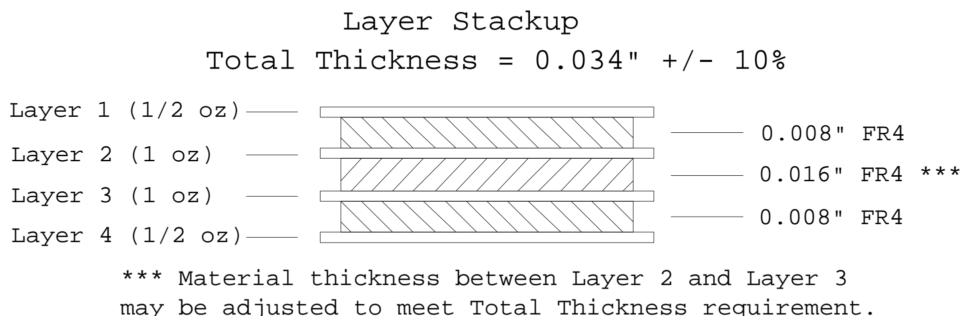
A properly designed PCB is essential to the operation of the EM250. Ember recommends that you closely adhere to the layout guidelines presented in the following sections. You can download the complete set of PCB layout files from the Ember support website (http:\\support.ember.com).

PCB overview (4 layers)

All 4-layer reference designs are based on either 0.062-inch-thick or 0.8mm-thick RoHS-compliant FR-4 board material. The layer stackup for each is defined in Figure 19. Note that all copper thicknesses can be either 1 or ½ ounce.



(a) Total Thickness 0.062"



(b) Total Thickness 0.8mm

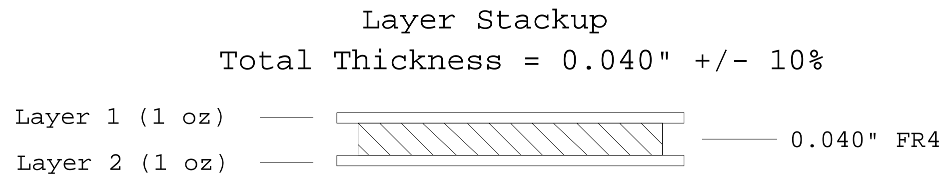
Figure 19. Fabrication stackup for the 4-layer reference designs

- **Layer 1**: The top layer is used for the majority of signal routing and all RF signal routing
- **Layer 2**: Ground layer with minimal signal routing
- **Layer 3**: Power distribution layer
- **Layer 4**: The bottom layer is used for signal routing and ground

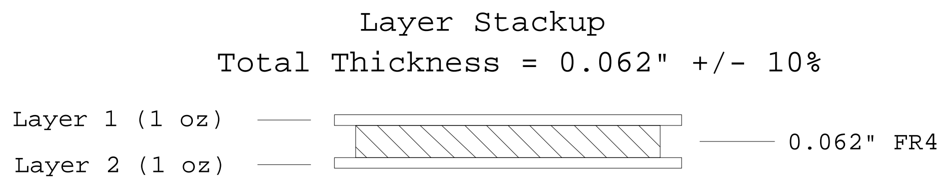
Design parameters such as trace width, trace spacing, and drill sizes were all selected so that the PCB could be fabricated using a low-cost standard process.

PCB overview (2 layers)

The layer stackup for each of the two layer reference designs are defined in Figure 20. Note that all copper thicknesses can be either 1 or ½ ounce as this has minimal effect on the controlled impedance.



(a) Layer Stack up for the 0.040" 2-Layer design



(b) Layer Stack up for the 0.062" 2-Layer design

Figure 20. 2-layer stack up

- **Layer 1**: The top layer is used for the majority of signal routing and all RF signal routing
- **Layer 2**: The bottom layer is used for signal routing and ground. As few traces as possible should be routed on this layer.

Design parameters such as trace width, trace spacing, and drill sizes were all selected so that the PCB could be fabricated using a low-cost standard process.

General layout guidelines

This section details the general PCB Layout guidelines to be followed on all of Ember's reference designs unless explicitly stated otherwise. Pertinent examples are given where required.

Grounding and power supply decoupling must be implemented properly on RF PCB designs. All decoupling capacitors should be small surface-mount components (preferably size 0402) and should be placed as close as possible to the supply pins, as shown in Figure 21.

To maximize the decoupling effectiveness, the capacitors should be placed between the supply pins and the vias to the internal power layer (Layer 3). Avoid placing vias between the supply pin and the capacitor.

To reduce parasitic inductance, all connections to the ground plane should be as short as possible through individual ground vias. If possible, do not route multiple ground connections through the same via.

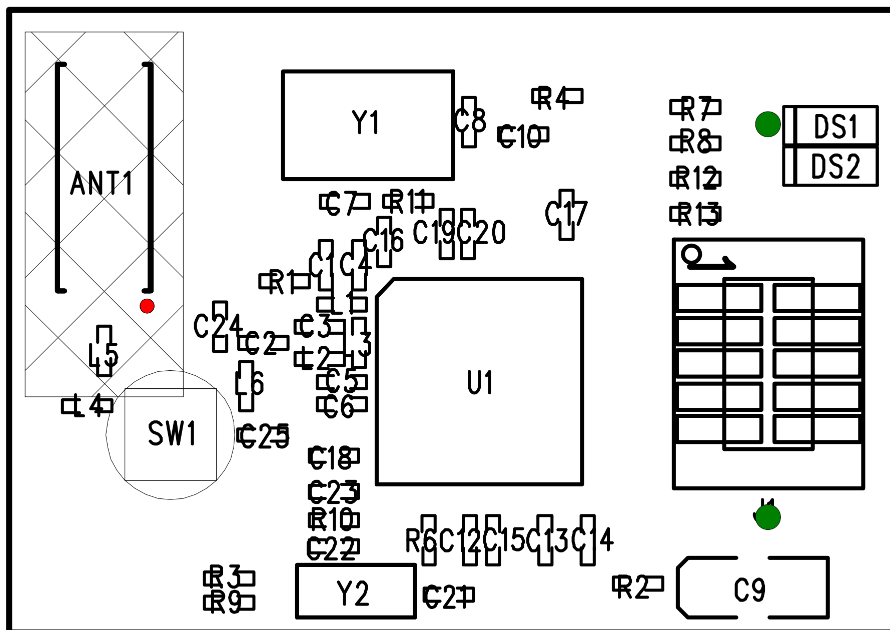


Figure 21. Top layer assembly print of the EM250 designs (Layer 1)

Traces between the 24MHz crystal and the EM250 should be short and direct. The loading capacitors and shunt resistor should be placed in line with those traces and kept symmetric. Ember recommends that the loading capacitors for the 24MHz crystal share a ground via.

In addition, Ember recommends the designer use a controlled impedance microstrip line to connect the single-ended port of the balun to the RF connector (or antenna, for applications where a connector is not used). The microstrip trace width is determined based on several parameters, including desired impedance, ground plane separation, and dielectric constant of the PCB substrate. Because the separation between the top layer (Layer 1) and the ground layer (Layer 2) is 0.008”, the microstrip trace width is 14 mils.

Balun and harmonic filter layout

As mentioned earlier in the section about the RF balun, the designer needs to choose between the ceramic or lattice balun architectures. To maximize performance of the RF design, the layout considerations outlined in this section should be strictly adhered to.

Ceramic balun and harmonic filter

The performance of the RF layout (ceramic balun and harmonic filter) is extremely sensitive to layout, and Ember strongly recommends that any layout involving the ceramic balun follow these guidelines:

- L1 should be a 0603 and placed as close to the EM250 RF pins as possible.
- The RF traces from the EM250 to the ceramic balun should be routed to the balun first, then to the inductor. This trace width should be 0.007” for 200-Ohm impedance.

- The balun decoupling capacitor should be placed as close to the balun as possible.
- If a bend is required in the controlled impedance microstrip, the bend should be mitered at 45°.

As mentioned earlier, the routing from the balun to the harmonic filter and antenna should be 50 ohm controlled impedance microstrip. Figure 22 demonstrates a layout that follows these guidelines. Note that the miter bends in the microstrip trace were implemented due to board size constraints.

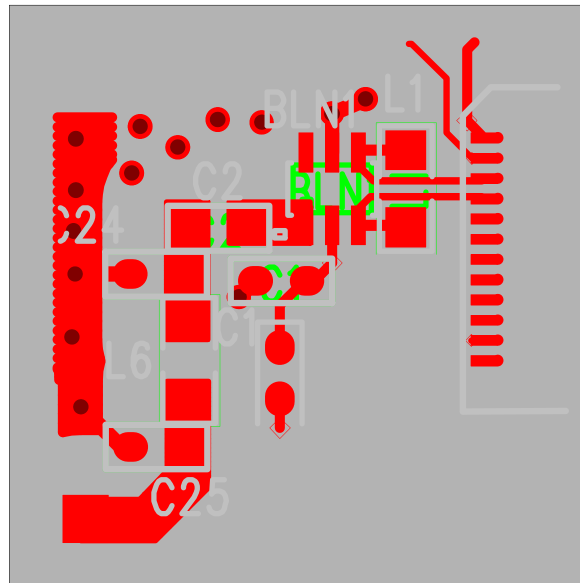


Figure 22. RF layout of the ceramic balun and harmonic filter reference design

Lattice balun and harmonic filter

The performance of the RF layout (lattice balun and harmonic filter) is extremely sensitive to layout, and Ember strongly recommends that any layout involving the lattice balun follow these guidelines:

- All balun components should be as compact and close to the EM250 RF pins as possible.
- C3 and L2 should be a 0402 and placed in parallel as close to the pads of L3 as possible.
- C5 and L1 should be a 0402 and placed in parallel to each other and as close to the pads of L3 as possible.
- Each ground connection should have its own via.
- The decoupling capacitor, C1, should be placed as close to the balun as possible.

These guidelines are illustrated in Figure 23.

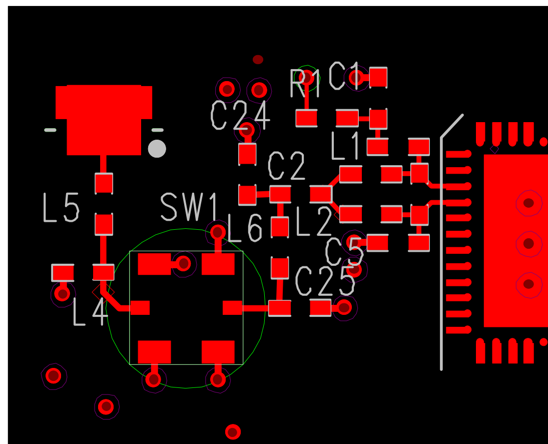


Figure 23. Lattice balun layout with harmonic filter

Ground vias

The EM250 requires the 49th pin to be attached to ground. Ember recommends that this connection be done through an array (3 x 3) of vias. These vias provide an electrical connection as well as a thermal relief point. This is illustrated in Figure 24.

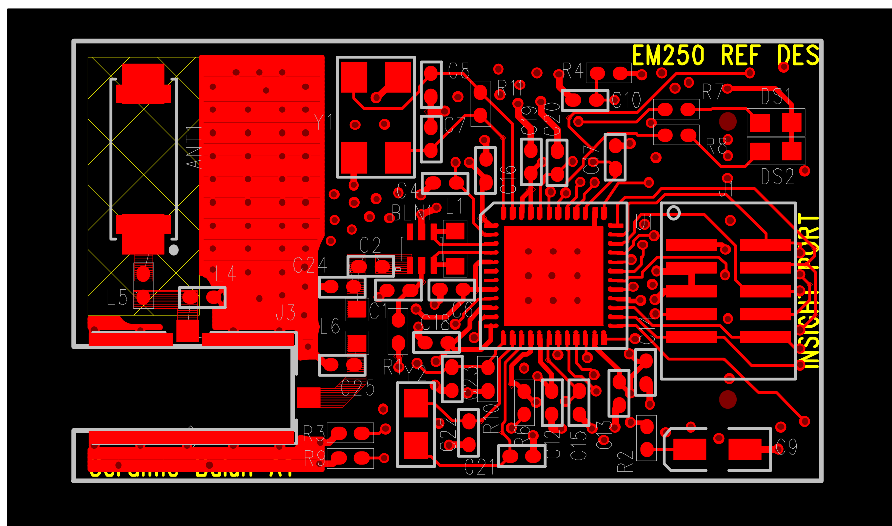


Figure 24. Layer 1 illustrating ground vias under the EM250

You should place additional ground vias on Layer 1 between the antenna and the crystal to “stitch” the ground points area to the internal ground plane (see Figure 24). This will prevent unwanted resonances from occurring, which could potentially affect RF performance.

After Reading This Document

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