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N10 OpenCPU
Features and Resources

Version 1.0

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GET CONNECTED GET SMART

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Notice

This document provides guide for users to use the N10 OpenCPU.

This document is intended for system engineers (SEs), development engineers, and test engineers.

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Revision Record		
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1 OpenCPU Features

1.1 Software Architecture

Figure 1-1 Software architecture

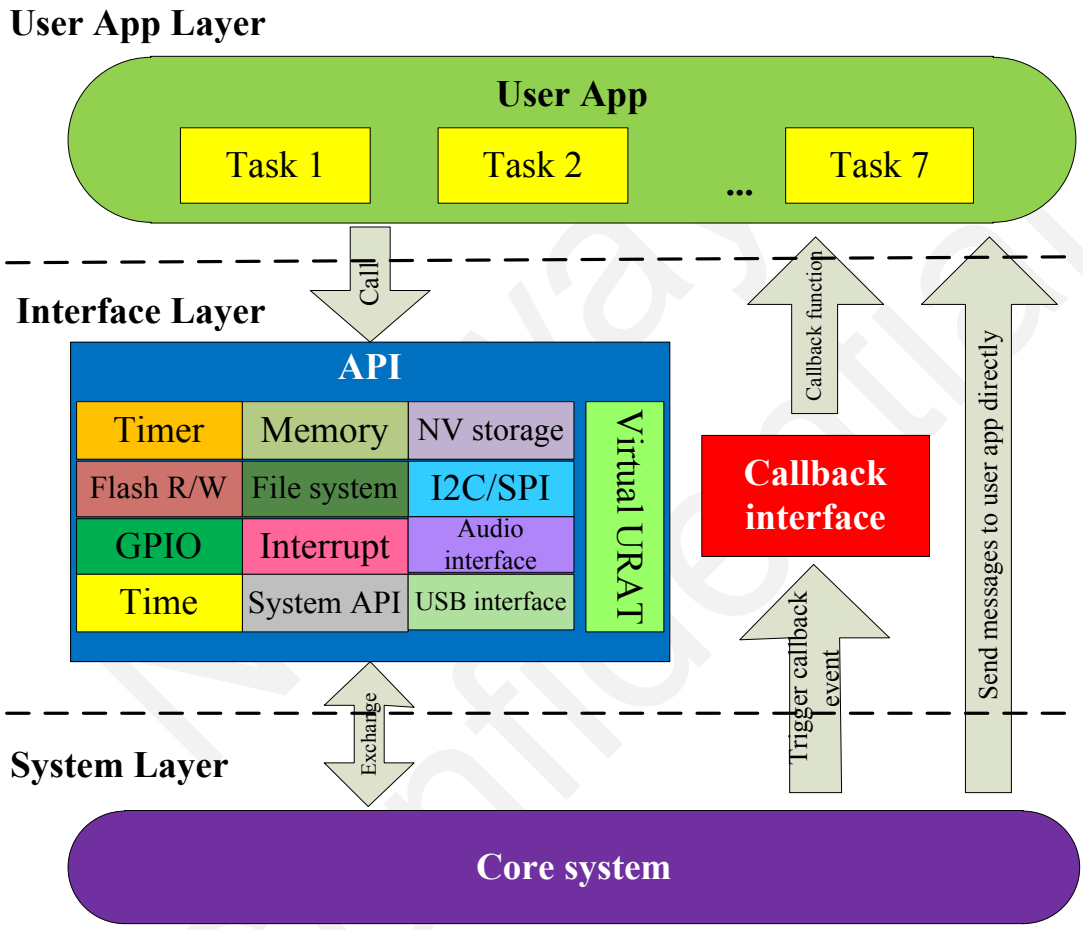

Figure 1-1 shows the architecture of the N10 OpenCPU platform.

This platform consists of three layers: core system layer, interface layer, and user app layer. This architecture allows users to conduct project development more flexibly and effectively so that they can save manpower during development. The system layer involves drivers, which are mainly used to call functions and communicate for the programs of the interface layer. To facilitate user development, some interfaces of the system layer are open to users. The interface layer includes GPIO configuration interface, interrupt interface, I2C interface, SPI interface, memory operation interface, NV memory interface, Flash read and write interface, timer interface, system callback interface, file system interface, audio interface, USB interface, and system interface. All these interfaces are open to users and can meet most requirements for project development. The user app layer includes task 1, task 2, to task 7, and user apps.

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User apps can call interfaces of the interface layer that are open to undertake local development more effectively and conveniently.

1.2 Software Features

- Seven default task
- Memory application and release
- NV parameter read and write
- Flash read and write
- Timer
- System clock
- GPIO control
- I2C control
- Configurable external interrupt
- File system
- TCP/IP
- Debugging print
- Remote upgrade
- All functions can be completed via AT commands

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2 OpenCPU Resources

Resources	Model
CPU	32-bit ARM7EJ-STM RISC 270 MHz
User task	7
UART	2
Memory	50 KB
NV	512 Bytes
FLASH	4 KB
Space between user code and data	200KB
Timer	31
System clock	Year/month/day/hour/minute/second
GPIO	22
I2C	1
Interrupt	9
File system	300 KB

CAUTION

- Some GPIO are multiplexed as I2C, UART2, VCCIO, and RING.
- DTR and LIGHT are multiplexed with some interrupts
- For more information, refer to 3 Hardware IO.

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3 Hardware IO Table

PA Pin No.	PA Pin Function	Corresponding MTK6261 PIN	Corresponding MTK6261 PIN
6	RX2	B2	RXHB
7	RX3	A1	RXLB
16	CTR1	A9	BPI_BUS2
17	CTR0	B9	BPI_BUS0
18	TXEN	B8	BPI_BUS1
19	RAMP	M8	APC
23	DCSIN	D2	TX_HB
24	GSMIN	C1	TX_LB

Truth Table				
	CTR1	CTR0	TXEN	RAMP
Default	0	0	0	-
Power Down	0	0	0	
GSM TX On	1	0	1	-
DCS TX On	1	1	1	-
RX2 On	1	0	0	-
RX3 On	1	1	0	-

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