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N1 Smart Module
I2C Configuration

Version 1.0

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Notice

This document provides guide for users to use the N1.

This document is intended for system engineers (SEs), development engineers, and test engineers.

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Change History		
Issue	Changes	Date
V1.0	Initial version	2016-08

Contents

1 Overview

I2C configuration includes two parts: DTSI configuration and clock configuration. This document describes how to configure I2C by taking sensor for instance.

2 DTSI Configuration

Add I2C configurations to the **soc** node.

File: N1_msm8909.dtsi

Location: kernel\arch\arm\boot\dts\jsr

```
i2c_1: i2c@78b5000 { /* BLSP1 QUP1 */
    compatible = "qcom,i2c-msm-v2";
    #address-cells = <1>;
    #size-cells = <0>;
    reg-names = "qup_phys_addr";
    reg = <0x78b5000 0x1000>;       ---A. I2C address
    interrupt-names = "qup_irq";
    interrupts = <0 95 0>;          ---B. Interrupt ID
    clocks = <&clock_gcc clk_gcc_blsp1_ahb_clk>,   ---C. Clock Configurations
            <&clock_gcc clk_gcc_blsp1_qup1_i2c_apps_clk>;
    clock-names = "iface_clk", "core_clk";
    qcom,clk-freq-out = <100000>;         ---D. Frequency control
    qcom,clk-freq-in  = <19200000>;
    pinctrl-names = "i2c_active", "i2c_sleep";   ---E. Pin control
    pinctrl-0 = <&i2c_1_active>;
    pinctrl-1 = <&i2c_1_sleep>;
    qcom,noise-rjct-scl = <0>;
    qcom,noise-rjct-sda = <0>;
    dmas = <&dma_blsp1 4 64 0x20000020 0x20>,
        <&dma_blsp1 5  32 0x20000020 0x20>;
    dma-names = "tx", "rx";
    qcom,master-id = <86>;
};
```


2.1 Determining I2C Address and Interrupt ID

Sensor adopts QUP1 and the I2C address is 0x78b5000 while the interrupt ID is 95 according to the Qualcomm documents.

Table 2-1 QUP physical address

BLSP Hardware ID	QUP Core	Physical Address
BLSP1	BLSP 1 QUP 1	0x78B500
BLSP1	BLSP 1 QUP 2	0x78B600
BLSP1	BLSP 1 QUP 3	0x78B700
BLSP1	BLSP 1 QUP 4	0x78B800
BLSP1	BLSP 1 QUP 5	0x78B900
BLSP1	BLSP 1 QUP 6	0x78BA00

Table 2-2 QUP IRQ

BLSP Hardware ID	QUP Core	IRQ
BLSP1	BLSP 1 QUP 1	95
BLSP1	BLSP 1 QUP 2	96
BLSP1	BLSP 1 QUP 3	97
BLSP1	BLSP 1 QUP 4	98
BLSP1	BLSP 1 QUP 5	99
BLSP1	BLSP 1 QUP 6	100

2.2 Configuring Pins

```
pmx_i2c_1 {        /* CLK, DATA */
    qcom,pins = <&gp 6>, <&gp 7>;
    qcom,num-grp-pins = <2>;
    qcom,pin-func = <3>;
    label = "pmx_i2c_1";

    i2c_1_active: i2c_1_active {
        drive-strength = <2>; /* 2 MA */
        bias-disable = <0>; /* No PULL */
    };

    i2c_1_sleep: i2c_1_sleep {
        drive-strength = <2>; /* 2 MA */
        bias-pull-down; /* PULL DOWN */
    };
};
```

MSM8909 adopts pinctrl to manage the status of pins.

Here you need to configure IO, the pins used and pin state (active or sleep).

3 Clock Configuration

```
clocks = <&clock_gcc clk_gcc_blsp1_ahb_clk>,   ---C. Clock configurations
            <&clock_gcc clk_gcc_blsp1_qup1_i2c_apps_clk>;
```

Clock source includes: clk_gcc_blsp1_ahb_clk, clk_gcc_blsp1_qup1_i2c_apps_clk

Select QUP to be configured and target: i2c.